AMENDMENTS TO THE CLAIMS

1-40 (Canceled)

41. (New) A method for defining a system specification for a digital system, said method comprising the steps of:

partitioning said system into a plurality of processes, each of the processes having a defined behavior and each of the processes having at least one control thread;

defining separately from said processes a single data independent data communication protocol for communication within said digital system and between said processes;

configuring data communication interfaces in the form of communication input ports and communication output ports for each of the processes, the communication ports forming memory free communication channels; and

combining the results of the steps of partitioning, defining and configuring to define specifications for said plurality of processes to form said system specification.

42. (New) The method of Claim 41, wherein the specification for a first process is independent of the specification of a second process.

43. (New) The method of Claim 41, further comprising the step of duplicating the specification for a process of a first system for a process of a second system.

44. (New) The method of Claim 41, wherein said step of configuring data communication interfaces involves defining communication interfaces with input ports and output ports to provide unidirectional, point-to-point connections between input ports of a first process and output ports of a second process, said input ports and said output ports being part of the associated processes.

45. (New) The method of Claim 44, wherein defining interfaces having input ports comprises the steps of:

defining a data terminal having a plurality of input signal lines;

defining a strobe terminal having at least one input signal line; and

defining an acknowledge terminal having at least one output signal line.

46. (New) The method of Claim 44, wherein defining interfaces having output ports comprises the steps of:

defining a data terminal having a plurality of output signal lines;

defining a strobe terminal having at least one output signal line; and

defining an acknowledge terminal having at least one input signal line.

47. (New) The method of Claim 44, further comprising of step of defining said processes to synchronize at communication instants.

48. (New) The method of Claim 44, wherein said ports are defined with a blocked protocol whereby the control flow of a process is halted until the process associated with the port is synchronized.

49. (New) The method of Claim 45, wherein said ports are defined with an unblocked protocol whereby the control flow of a process continues regardless of whether the process associated with the port is synchronized.

50. (New) The method of Claim 44, wherein the communication protocol comprises a four-phase handshake protocol.

51. (New) The method of Claim 44, wherein said step of partitioning comprises defining a plurality of processes as a single process.

52. (New) The method of Claim 44, wherein said processes are implemented in a hardware description language or in a programming language.

53. (New) The method of Claim 52, wherein said processes are implemented in C, Silage or VHDL language.

54. (New) A method of implementing a digital system comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;

defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;

organizing said data communication protocol with input and output ports for said processes, said ports using memory free communication channels; and

designing a plurality of processors to implement said process.

55. (New) The method of Claim 54, wherein said step of designing processors comprises the step of specifying a processor having specification which conform to the processes implemented.

56. (New) The method of Claim 55, wherein said processor comprises a programmable, general purpose processor.

57. (New) The method of Claim 55, wherein said processor comprises a programmable digital signal processor.

58. (New) The method of Claim 55, wherein said processor comprises a dedicated, custom processor.

59. (New) The method of Claim 55, wherein said processor comprises custom logic circuitry with a controller such that the resulting digital system operates according to functional and real-time specifications.

60. (New) The method recited in Claim 55, wherein said ports and communication channels are implemented as shared memory.

61. (New) The method recited in Claim 55, wherein said ports and communication channels are implemented as sockets.

62. (New) The method recited in Claim 55, wherein said ports and communication channels are implemented as files.

63. (New) The method recited in Claim 55, wherein said ports and communication channels are implemented as a mailbox.

64. (New) The method recited in Claim 55, wherein said ports and communication channels are implemented in the operating system of a multi-process operating system for simulating the system processes and communications channels on a network of computers.

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66. (New) The method recited in Claim 55, wherein said ports and communication channels are implemented in the operating system of a multi-process operating system for simulating the system processes and communications channels in a multi-tasking implementation shell.

67. (New) The method of Claim 55, wherein said communication ports connect processes defined of at least one of a plurality of specifications.

68 (New) The method of Claim 57, wherein said plurality of specifications are selected from a group consisting of Silage descriptions, C descriptions, VHDL process descriptions.

69. (New) The method of Claim 55, wherein said communication channels are implemented as memory mapped I/O.

70. (New) The method of Claim 55, wherein said communication channels are implemented as interrupt driven I/O.

71. (New) The method recited in Claim 56, wherein said communication channels are implemented in integrated circuit form for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types.

72. (New) The method of Claim 71, wherein said plurality of processor types consists of Cathedral-III processors, ARM processors and VHDL generated processors.

73. (New) The method recited in Claim 56, wherein said communication channels are implemented in software for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types.

74. (New) The method recited in Claim 56, wherein said communication channels are implemented in a combination of hardware and software, for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types.

75. (New) The method recited in Claim 57, wherein said step of partitioning involves defining a library of auxiliary processes to simulate the digital system, the library of processes selected from a plurality of processes.

76. (New) The method of Claim 75, wherein said plurality of processes consists of one or more of an interactive I/O process, a file I/O process, a graphical output process, a channel duplicator process, a channel merging process, a FF. process, a slider process, a button process, a first-in, first-out buffer process, an ARM processor, a digital to analog conversion process and an analog to digital conversion process.